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10/070,008	07/03/2002	Gilbert Wolrich	10559-311US1	5753

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Fish & Richardson
225 Franklin Street
Boston, MA 02110-2804

EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/070,008	WOLRICH ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-14 and 17-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-14 and 17-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/09/04, 02/28/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-4,6,7-14,17-23 remain for examination. Claims 24-26 have been added. Claims 5,15,16 have been canceled.

2. Kitta (5,394,530), Chrysos et al. (5,923,872), and Brodnax et al. (5,463,746) are newly cited art.

3. Hasegawa (5,724,563), (5,394,530), Khim Yeoh et al. (5,274,770), and Brucker et al. (4,742,451) were cited on the record, therefore, copies are not included.

4. This action includes new ground of rejections to newly amended claims 1, 23-26.

5. Applicant's arguments with respect to claim1 have been considered but are moot in view of the new ground(s) of rejection. To clarify the issue, response to applicant's remarks on 08/08/05 will be addressed below :

6. In the remarks, applicant argued that :

a) Hasegawa does not disclose, suggest or even mention the combination of a first token that specifies the nùmber of instructions after the branch instruction to execute before performing the branch operation and a second token that specifies a branch guess operation;

b) Hasegawa neither describes nor suggests executing a branch instruction that causes a branch operation in an instmction strenm based on any specified value being true or false as recited in claim 17 .

7. As to a) above, see disccussions set forth in paragraphs 2,3,and 10,11.

8. As to b), Hasegawa taught execution of a branch instruction that caused a branch operation in an instmction strenm based on any specified value being true or false (see the condition comparisons in col.11, lines 21-54 for the true and false determination).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1,17,19-22 are rejected under 35 U.S.C. 102(a) and (b) as being anticipated by Hasegawa (5,724,563).

10. As to newly amended claim 1, claim 1 is rejected under the interpretation of the guess token is a conditional code, such as Zero, Carry, Oveflow etc.

11. As to claim 1, Hasegawa disclosed a computer system including at least :

a) a branch instruction (Branch) that caused a branch in execution of an instruction stream (instruction at the target address and the sequence) based on any specified value being true or false and including a first token that specified number of instructions in an instruction stream that were after the branch instruction (see the instructions

following the Branch, see the field for the number of instructions specified in the branch instruction format in fig.2) to execute before the branch operation (see also the number of successive instructions designated by the predictive branch before the branch control flow was changed in col.3, lines 25-30, lines 55-59, col.9, lines 29-33, col.12, lines 37-46, see figs.5, 10B Branch after 3 to X , Branch after 3 to X, Branch after 4 to X, see the decision on branch condition in col.1, lines 19-22 for the background teaching of true or false, see also col.1 1, lines 14-24, col.12, lines 6-13 for judging a branch condition), and a second token specifying a branch guess operation (see the conditional codes in col.11, lines 20-52.

12. As to the deferring of the branch performance based' on the token specifying number of instructions in claim 17, Hasegawa also included deferring the branch operation based on the token number specified in instruction (see the branch instruction format in 2, see the field for storing the number of instructions, see also fig.5, and fig.10B, and fig.5B the numerical value 3, or the counter value counting down the order of instructions , see also the number 3 and 4 in the branch instruction in fig.10B) .

13. As to claim 22, Hasegawa also taught processor comprising:

a) decode logic for decoding instructions (see decoding section in col.6, lines 43-50), the decode logic including logic to execute a branch instruction in execution of an instruction stream in the processor, with a branch operation based on any specified value in the branch instruction being true or false (se the conditional comparison in col.11, lines 20-54) and including a token that specifies the number of instructions in the instruction stream to execute before performing the branch operation (see the number

of instructions after the branch specified in the instruction field in fig.2, see also the number of instructions after branch in col.6, lines 25-32).

14. As to claim 21, Hasegawa did not explicitly show assembler program as clamed. However, since no specific type of assemble program ahs been reflected into the claim, the assemble is read as any general type of assembly program. Therefore, the examiner holds that Hasegawa should have included assembler program in general because the branch prediction of Hasewaga was directed to the bit level of the condition codes (see the Z, O, C bits in col.6, lines 20-54). In addition, Hasegawa did show a compiler top fill the delay cycles (see col.3, lines 20-24).

15. As to claims 19,20, Hasegawa was also directed to efficiency of program coding (see the application program in col.1, lines 42-48 , col.3, lines 25-32 for background).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 1-4,6-9,11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa (5,724,563) In view of Kitta (5,394,530).

17. Claim 1 is also alternatively rejection under the 35 U.S.C. 103(a) based on different interpretation .

18. As to claims 1 ,4, Hasegawa disclosed a computer system including at least : a) a branch instruction (Branch) that caused a branch in execution of an instruction stream (instruction at the target address and the sequence) based on any specified value being true or false and including a first token that specified number of instructions in an instruction stream that were after the branch instruction (see the instructions following the Branch, see the field for the number of instructions specified in the branch instruction format in fig.2) to execute before the branch operation (see also the number of successive instructions designated by the predictive branch before the branch control flow was changed in col.3, lines 25-30, lines 55-59, col.9, lines 29-33, col.12, lines 37-46, see figs.5, 10B Branch after 3 to X , Branch after 3 to X, Branch after 4 to X, see the decision on branch condition in col.1, lines 19-22 for the background teaching of true or false, see also col.1 1, lines 14-24, col.12, lines 6-13 for judging a branch condition).

19. Hasegawa did not specifically show the second token for specifying a branch guess operation as claimed. However, Kitta disclosed that it was known in the art to guess in order to overcome the potential loss of cycle, using BHT as to which instruction specified by a branch target address is to be applied to the execution unit (see col.1, lines 23-27). It would have been obvious to one of ordinary skill in the art to use Kitta in Hasegawa for including the second token for specifying a branch guess operation as claimed because the use of Kitta could provide Hasegawa the control

ability to predict the branch at a predefined format , thereby reducing the latency of the branch prediction, and because Hasewaga also disclosed a branch judging circuit for determining the condition of the branch on the predictive branch instruction (see col.11, lines 20-52), which was a suggestion of need of using a guess token for branch operation, for purpose of enhancing the result of the predictive branch conditions, and in doing so , provided a motivation.

20. As to claim 2, Hasegawa also included a branch guess operation (x).

21. A to claim 3 Hasegawa also included execution of the instruction branched, and the number of the instruction to be executed (see fig.5A)

22. As to claims 6,7, Hasegawa was also directed to efficiency of program coding (see the application program in col.1, lines 42-48 , col.3, lines 25-32 for background).

23. As to claims 8, Hasegawa also included unconditional branch (see col.5, lines 50-53) and ALU conditional branch (see the arithmetic flags in col.1 1, lines 19-52).

24. As to claim 9, see branch condition bit c,v in col.1 1 , lines 25-32).

25. As to claim 11, Hasegawa also included a specified context (see the number of instructions 3 in the Branch after 3 X in fig.5).

26. As to claim 12, Hasegawa included a selected state name of a selected value (see the opcode value in Table 1 col.1 1).

27. As to claim 13, Hasegawa also deasserted a specified signal (see the "0" or "1" in the flag in col.1 1 , lines 32).

28. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa (5,724,563) in view of kitta (5,394,530) and as applied to claim 1 above, and further in view of Khim Yeoh et al. (5,274,770).

29. As to claim 10, limitation of the parent claim 1 have been discussed in previous paragraph , therefore, it will not be repeated herein. Neither Hasegawa nor kitta specifically showed the match or mismatch of the byte compare value as claimed. Hasegawa disclosed a comparison of arbitrary bit number of an opcode in a long word (see the branch instruction) with a 4 bit compare value (see the judgment of the condition code based on the opcode in tol.1 1, lines 19-40). Hasegawa's condition code included only 4 bits. However, Khim Yeoh disclosed a system for performing a conditional branch based a comparison of values in bytes (see col.3, lines 15-18). It would have been obvious to one of ordinary skill in the ad to use Khim Yeoh in Hasegawa for including the match and mismatch (i.e. comparison) of the byte compare value as claimed because the use of Khim Yeoh could expand the processing structure of Hasegawa to accept additional conditional parameters, such as the conditional code of more than 4 bits, thereby enhancing the adaptability of the system status, and because one of ordinary skill in the art should be able to recognize the arbitrary bit number (e.g. 3, 4,8,16 etc.) of the conditional opcode in Hasegawa could also be

applicable in the condition code to increase the bit width, and for the above reasons provided a motivation.

30. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa (5,724,563) in view Kitta (5,394,530) as applied to claim 1 above, and further in view of Brucker et al. (4,742,451).

31. As to claim 14, Hasegawa did not specifically showed the prefetch of the instruction for the branch taken condition as claimed. However, Brucker disclosed a conditional branch system including a prefetch of instruction for a branch taken (see the prefetch in col.7, lines 28-33, lines 34-53). It would have been obvious to one of ordinary skill in the art to use Brucker in Hasegawa for perfecting the instruction for the branch taken as claimed because the use of Brucker could provide additional capability to adapt to specific processing requirement, such as the branch prediction, of the branch instruction in Hasegawa, thereby reducing the repeated cycle of branch result, and therefore, increasing the overall time of the branch processing, and it could be readily achieved by predefining the control tokens of branch prediction in Brucker , such as prefetch on taken , not taken, into the configuration file of Hasegawa so that the specific branch prediction could be recognizable by Hasegawa in order to achieved the enhanced processing performance, ion doing so, provided a motivation. Hasegawa is used as primary reference because it shoed clearly the number of instructions specified in the branch instruction. Brucker is used to supplement the teaching of the prefetch for branch taken.

32. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa (5,724,563) in view of Brucker et al. (4,742,451).

33. As to claim 18, limitation of parent claim 17 has been discussed in paragraph 12 above. Hasegawa did not specifically showed the prefetch of the instruction for the branch taken condition as claimed. However, Brucker disclosed a conditional branch system including a prefetch of instruction for a branch taken (see the prefetch in col.7, lines 28-33, lines 34-53). It would have been obvious to one of ordinary skill in the art to use Brucker in Hasegawa for perfecting the instruction for the branch taken as claimed because the use of Brucker could provide additional capability to adapt to specific processing requirement, such as the branch prediction, of the branch instruction in Hasegawa, thereby reducing the repeated cycle of branch result, and therefore, increasing the overall time of the branch processing, and it could be readily achieved by predefining the control tokens of branch prediction in Brucker , such as prefetch on taken , not taken, into the configuration file of Hasegawa so that the specific branch prediction could be recognizable by Hasegawa in order to achieved the enhanced processing performance, ion doing so, provided a motivation. Hasegawa is used as primary reference because it shoed clearly the number of instructions specified in the branch instruction. Brucker is used to supplement the teaching of the prefetch for branch taken.

34. Claims 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa (5,724,563) in view of Chrysos et al. (5,923,872).

35. As to claims 24-26, limitations of claim 22 were already discussed in paragraph 13 above. Hasegawa did not specifically teach the hardware based multi threaded as claimed. However, Chrysos disclosed a system including hardware contexts for simultaneously multithreaded execution (see col.12, lines 15-18). It would have been obvious to one of ordinary skill in the art to use Chrysos in Hasegawa for including the hardware based multi threaded as claimed because the use of Chrysos could provide Hasegawa the capability to adjust to specific hardware construct of the branch prediction, and it could be readily achieved by configuring the hardware parameters of Chrysos (or the contexts) into Hasegawa so that the specific hardware based multithreads of Chysos could recognized by Hasegawa, and because Hasegawa was also directed to the reduction of the delay cycles of the pipelined branch instructions (see col.3, lines 1-24), which was a suggestion of the need for including multiple executable threads in order to achieve the efficiency of the pipelined process in Hasegawa, for the above reason, provided a motivation. As to the hardware base , see the bit level of the condition codes in fig.9.

36. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa (5,724,563) in view of Brodnax et al. (5,463,746).

37. As to claim 23, limitations of claim 22 have been discussed in paragraph 13. Hasegawa did not specifically teach the guess token for the branch operation as claimed. However, Brondnax disclosed a guess branch token (see fig.4 [GUESS], see also col.4 , lines 26-43 for the guess bit embedded into the branch instruction). It would

have been obvious to one of ordinary skill in the art to use Brodnax in Hasegawa for including the branch token as claimed because the use of Brodnax could provide Hasegawa the capability to speculate the target instruction in a given instruction, and therefore, eliminating hardware overheads of the circuit , and because Hasewaga also disclosed a branch judging circuit for determining the condition of the branch on the predictive branch instruction (see col.11, lines 20-52), which was an indication of the demand for using predictive information, such as a flag or bit for branch guess operation, in order to reduce the latency due to the circuit overheads of the predictive branch conditions, and therefore, provided a motivation.

Applicant's amendment (to claims 1, 23-26) necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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